What is claimed is

1. Field effect transistor comprising:

a substrate having a doping of a first conductivity type;

a drain area in the substrate having a doping of a second conductivity type opposite to the first conductivity type;

a source area in the substrate being laterally spaced from the drain area and having a doping of the second conductivity type;

a channel area in the substrate that is arranged between the source area and the drain area; and

an area having a doping of the second conductivity type and connected to the drain area and arranged in a portion of the substrate adjacent to the drain area such that alternating regions having the first conductivity type and having the second conductivity type are disposed in the portion.

2. Field effect transistor of claim 1, wherein the area is formed so that the portion of the substrate bordering the drain area is completely depleted upon applying a predetermined drain voltage.

3. Field effect transistor of claim 1, wherein the area comprises a comb-shaped cross section.

4. Field effect transistor of claim 1, wherein the substrate comprises a surface at which the source area, the channel area, and the drain area are arranged, and wherein the area comprises one or a plurality of lamellae or columns arranged in parallel or perpendicular to the surface of the substrate.

5. Field effect transistor of claim 1, wherein the substrate comprises a surface at which the source area, the channel area, and the drain area are arranged, and wherein the portion of the substrate in which the area is arranged is disposed at a side of the drain area facing away from the surface of the substrate.

6. Field effect transistor of claim 1, wherein the substrate comprises a base substrate having a surface and an epitaxial layer epitaxially grown on the surface of the base substrate, wherein the source area, the drain area, and the channel area being arranged in the epitaxial layer, and the portion in which the area is arranged extending from the drain area to the surface of the base substrate.

7. Field effect transistor of claim 1, wherein the drain area includes a low-doped drain sub-area having one or more drain portions in which a doping concentration in direction to the channel area decreases continuously or stepwise.

8. Field effect transistor of claim 7, wherein a lateral expansion of the area is at least as great as a lateral expansion of the most highly doped portion of the drain area.

9. Field effect transistor of claim 1, wherein the field effect transistor is a LDMOS field effect transistor with a source area created by lateral diffusion.

10. Field effect transistor of claim 1, wherein the area is created by successive epitaxy and implantation.

11. Semiconductor chip with a field effect transistor according to claim 1.